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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
UMEZ ERONINI, LYNETTE T

ART UNIT	PAPER NUMBER
1765	6

DATE MAILED: 06/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

A 2-6

Office Action Summary	Applicati n No.	Applicant(s)	
	09/855,894	NING, XIAN J.	
	Examin r	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**.. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bigelow (US 4,657,629).

As pertaining to claims 1 and 2, Bigelow teaches, substrate **10** may comprise one or more layers of dielectric and interconnect metal (column 3, lines 42-45). Bigelow further teaches photoresist layer **14** is spin coated to cover the underlying semiconductor structure (column 3, lines 57-59), the entire surface **15** of photoresist layer **14** is exposed to UV at a prescribed energy density and time to completely expose the entirety of the thickness of layer **14** (column 3, lines 63-67), and the top layer of photoresist **16** is exposed to ultraviolet radiation **20** through a photolithographic mask **18** having an aperture pattern **19** (column 4, lines 15-19), which reads on,

A method of patterning metal layers of a semiconductor wafer, the method comprising:

depositing a first resist over the second conductive layer;

patterning the first resist with a first pattern;

depositing a second resist over the first resist; and

patterning the second resist with a second pattern.

Bigelow further teaches patterning of the second photoresist layer **16**, the entire structure is subjected to a reactive ion etch (column 4, lines 41-44) and this etching step etches both the top photoresist layer **16** and the underlying thick photoresist layer **14** and transfers the aperture pattern **21** in the top photoresist layer **16** into the thick photoresist layer **14** therebeneath (column 4, lines 41-48). Following complete etching through the pattern **21** into the underlayer **14** (column 4, lines 56-57), which reads on,

simultaneously transferring the first pattern to the first conductive layer and the second pattern to the second conductive layer.

Bigelow differs in failing to teach depositing a first conductive layer over a substrate; depositing an insulating layer over the first conductive layer; and depositing a second conductive layer over the insulating layer, in claim 1.

It is well known in the art that semiconductors are made of more than one dielectric and conductive layers.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Bigelow by using conventional semiconductors layers to make the semiconductor structure as claimed in the present invention for the purpose of patterning semiconductor having multi-levels.

Since Bigelow uses two photoresists in patterning dielectric and conductive layers as that of the claimed invention, then using Bigelow's photoresist processing method in the same process as that of the claimed invention would obviously result wherein the insulating layer comprises a capacitor dielectric, wherein transferring the first pattern to the first conductive layer comprises forming bottom metal plates of a MIM capacitor, and wherein transferring the second pattern to the second conductive layer, **as in claim 5**; and in transferring the first pattern to the insulating layer, **as in claim 6**.

3. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bigelow ('629) as applied to claim 1 above, and further in view of Lee et al. (US 4,592,132).

Bigelow differs in failing to teach the first resist comprises a negative resist and the second resist comprises a positive resist, in claim 3 and the first resist comprises a positive resist and the second resist comprises a negative resist, in claim 4.

Lee teaches the first and second layers **30** and **38** of photoresist may be both negative or both be positive (column 4, lines 51-53).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Bigelow by using Lee's negative and positive photoresists for the purpose of utilizing a combination of negative and positive photoresist polymers to build up the photoresist to a desired thickness, wherein the solvent in these respective photoresist material do not adversely

interact with each other and do not tend to dissolve the adjacent negative or positive material (column 2, lines 37-43).

4. Claims 7, 8, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Bigelow (US '629).

As pertaining to claims 7 and 8, Bigelow teaches, substrate **10** may comprise one or more layers of dielectric and interconnect metal (column 3, lines 42-45). Bigelow further teaches photoresist layer **14** is spin coated to cover the underlying semiconductor structure (column 3, lines 57-59), the entire surface **15** of photoresist layer **14** is exposed to UV at a prescribed energy density and time to completely expose the entirety of the thickness of layer **14** (column 3, lines 63-67), and the top layer of photoresist **16** is exposed to ultraviolet radiation **20** through a photolithographic mask **18** having an aperture pattern **19** (column 4, lines 15-19), which reads on,

A method of pattering metal layers of a semiconductor wafer,

depositing a first resist over the second conductive layer;

patterning the first resist with a first pattern;

depositing a second resist over the first resist.

Bigelow further teaches patterning of the second photoresist layer **16**, the entire structure is subjected to a reactive ion etch (column 4, lines 41-44) and this etching step etches both the top photoresist layer **16** and the underlying thick photoresist layer **14**, it transfers the aperture pattern **21** in the top photoresist layer **16** into the thick photoresist layer **14** therebeneath (column 4, lines 41-48), which reads on,

patterning the second resist with a second pattern.

Following complete etching through the pattern **21** into the underlayer **14** (column 4, lines 56-57), reads on,

simultaneously transferring the first pattern to the first conductive layer and transferring the second pattern to the second conductive layer, **in claim 7**; and

wherein transferring the first pattern to the first conductive layer and transferring the first and second pattern comprise exposing the wafer to a reactive ion etch process, **in claim 8**.

Bigelow differs in failing to teach, the wafer comprising a first conductive layer, an insulating layer disposed over the first conductive layer and a second conductive layer disposed over the insulating layer, in claim 7.

It is well known in the art that semiconductors are made of more than one dielectric and conductive layers.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Bigelow by using conventional semiconductors layers to make the semiconductor structure as claimed in the present invention for the purpose of patterning semiconductor having multi-levels.

Since Bigelow uses the same method of using two photoresists in patterning dielectric and conductive layers, then using Bigelow's photoresist processing method in the same process as that of the claimed invention would have obviously result in,

wherein the insulating layer comprises a capacitor dielectric, wherein transferring the first pattern to the first conductive layer comprises forming bottom metal plates of a

MIM capacitor, and wherein transferring the second pattern to the second conductive layer, **as in claim 11**; and further comprising transferring the first pattern to the insulating layer, **as in claim 12**.

Claim Rejections - 35 USC § 103

5. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bigelow ('629) as applied to claim 7 above, and further in view of Lee ('132).

Bigelow differs in failing to teach the first resist comprises a negative resist and the second resist comprises a positive resist, in claim 9 and the first resist comprises a positive resist and the second resist comprises a negative resist, in claim 10.

Lee teaches the first and second layers **30** and **38** of photoresist may be both negative or both be positive (column 4, lines 51-53).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Bigelow by using Lee's negative and positive photoresists for the purpose of utilizing a combination of negative and positive photoresist polymers to build up the photoresist to a desired thickness, wherein the solvent in these respective photoresist material do not adversely interact with each other and do not tend to dissolve the adjacent negative or positive material (column 2, lines 37-43).

6. Claims 13, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bigelow (US '629).

As pertaining to claims 13, 14, and 17, Bigelow teaches, substrate **10** may comprise one or more layers of dielectric and interconnect metal (column 3, lines 42-45). Bigelow further teaches photoresist layer **14** is spin coated to cover the underlying semiconductor structure (column 3, lines 57-59), the entire surface **15** of photoresist layer **14** is exposed to UV at a prescribed energy density and time to completely expose the entirety of the thickness of layer **14** (column 3, lines 63-67), and the top layer of photoresist **16** is exposed to ultraviolet radiation **20** through a photolithographic mask **18** having an aperture pattern **19** (column 4, lines 15-19), which reads on,

A method of forming capacitive plates of a MIM capacitor, comprising:

depositing a first resist over the second conductive layer;

patterning the first resist with a first pattern;

depositing a second resist over the first resist;

patterning the second resist with a second pattern.

Bigelow further teaches patterning of the second photoresist layer **16**, the entire structure is subjected to a reactive ion etch (column 4, lines 41-44) and this etching step etches both the top photoresist layer **16** and the underlying thick photoresist layer **14**, it transfers the aperture pattern **21** in the top photoresist layer **16** into the thick photoresist layer **14** therebeneath (column 4, lines 41-48). Following complete etching through the pattern **21** into the underlayer **14** (column 4, lines 56-57), which reads on,

simultaneously transferring the first pattern to the first conductive layer and transferring the second pattern to the second conductive layer.

Bigelow differs in failing to teach,

providing a wafer having a substrate; depositing a first conductive layer on the substrate; depositing a capacitor dielectric layer over the first conductive layer; and depositing a second conductive layer over the capacitor dielectric layer, in claim 11.

It is well known in the art that semiconductors are made of more than one dielectric and conductive layers.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Bigelow by using conventional semiconductors layers to make the semiconductor structure as claimed in the present invention for the purpose of patterning semiconductor having multi-levels.

Since Bigelow uses the same method of using a two photoresist in patterning dielectric and conductive layers, then if Bigelow's photoresist processing method is used in the same process as that of the claimed invention, then it would be obvious that using Bigelow's etching method would result in,

further comprising transferring the first pattern to the insulating layer, **as in claim 17**.

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bigelow ('629) as applied to claim 13 above, and further in view of Lee (US '132).

Bigelow differs in failing to teach the first resist comprises a negative resist and the second resist comprises a positive resist, in claim 15 and the first resist comprises a positive resist and the second resist comprises a negative resist, in claim 16.

Lee teaches the first and second layers **30** and **38** of photoresist may be both negative or both be positive (column 4, lines 51-53).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Bigelow by using Lee's negative and positive photoresists for the purpose of utilizing a combination of negative and positive photoresist polymers to build up the photoresist to a desired thickness, wherein the solvent in these respective photoresist material do not adversely interact with each other and do not tend to dissolve the adjacent negative or positive material (column 2, lines 37-43).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 703-306-9074. The examiner is normally unavailable reached on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703-308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

ltue
June 2, 2003

GEORGE GOUDREAU
PRIMARY EXAMINER